Claims

1.Transformer Circuit Arrangement
- with a first transformer with at least two inputs and at least two outputs and a first frequency response with a first lower limit frequency and a first upper limit frequency, and
- with a second transformer with at least two inputs and at least two outputs and a second frequency response with a second lower limit frequency and a second upper limit frequency,
- whereby the first lower limit frequency is smaller than the second lower limit frequency and the second upper limit frequency is greater than the first upper limit frequency,
- whereby at least one input of the first transformer is electrically connected to an input of the second transformer and at least one output of the first transformer is connected to an output of the second transformer, and
- whereby the frequency response of the transformer circuit arrangement has a bandpass behaviour with a lower overall limit frequency and an upper overall limit frequency, whereby the lower overall limit frequency is smaller than the first upper limit frequency and the second lower limit frequency, and the upper overall limit frequency is greater than the second lower limit frequency and the first upper limit frequency.

2. Transformer circuit arrangement according to Claim 1, wherein the first transformer has a first transformation ratio, a first main inductance, and a first scatter inductance, and wherein the second transformer has a second transformation ratio, a second main inductance, and a second scatter inductance.

3. Transformer circuit arrangement according to Claim 2, wherein the first transformation ratio is as great as the second transformation ratio.

4. Transformer circuit arrangement according to Claim 1, wherein the inputs of the transformers are connected in parallel or in series.

5. Transformer circuit arrangement according to Claim 1, wherein the outputs of the transformers are connected in series or in parallel.

6. Transformer circuit arrangement according to Claim 1, wherein a first capacitance is connected in parallel with the first transformer, downstream or upstream.

7. Transformer circuit arrangement according to Claim 1, wherein a second capacitance is connected in parallel with the second transformer, upstream or downstream.

8. Transformer circuit arrangement according to Claim 1, wherein the first frequency response and/or the second frequency response has a Butterworth behaviour.

9. Transformer circuit arrangement according to Claim 1, wherein the first frequency response and/or the second frequency response has a Butterworth behaviour of the second order.

10. Transformer circuit arrangement according to Claim 1, wherein the first transformer and/or the second transformer has an insertion loss of some 6dB at the individual lower and/or upper first or second limit frequencies respectively.

11. Transformer circuit arrangement according to Claim 1, wherein the first upper limit frequency is approximately the same as the second lower limit frequency.

12. Transformer circuit arrangement according to Claim 1, wherein the lower overall limit frequency is approximately

equal to the first lower limit frequency and/or the upper overall limit frequency is approximately equal to the second upper limit frequency.

13. Transformer circuit arrangement according to Claim 1, wherein an additional inductance is connected in series with the first transformer, upstream or downstream.

14. Transformer circuit arrangement according to Claim 1, wherein the transformer circuit arrangement is designed for the transfer of signals in message transmission systems.

15. Transformer circuit arrangement according to Claim 1, wherein the second lower limit frequency is not greater or smaller by a factor of 10 than the first upper limit frequency.

16. Transformer circuit arrangement according to Claim 1, wherein the first transformer and/or the second transformer is formed by a transformer circuit arrangement according to Claim 1.